The SOK Zynq® Target for MATLAB® Simulink® provides a new interface between Zynq hardware and the development level in MATLAB Simulink. This interface extends MATLAB so that the workflow in Simulink and the code generated from Simulink models is tailored specifically for Xilinx Zynq UltraScale+™ MPSoC products. In particular, this means that the SOK Zynq Target enables the use of MATLAB in combination with Zynq hardware and the following new features:

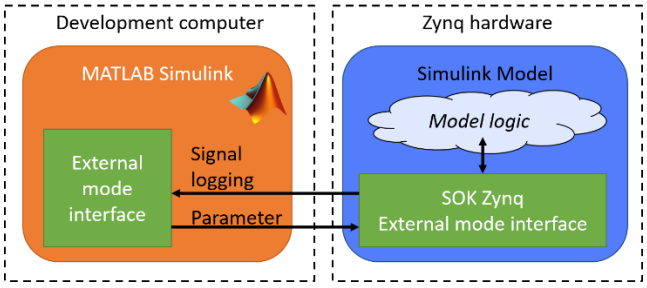
- Intuitive and extensive configuration settings
- MATLAB's external mode for FreeRTOS
- Internal real-time communication
- Integrated build process with Vitis™
- Simulink library blocks for external communication

These features are described in detail in the next paragraphs.

Concept of the SOK Zynq Target.

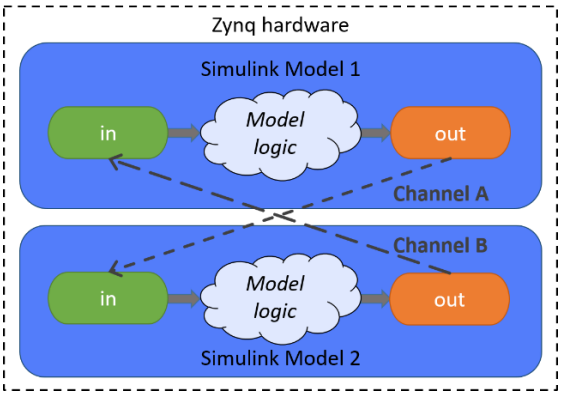
Once the target is installed and activated, **additional configuration options** for code generation of a Simulink model are accessible. For example, the new configuration options allow a user to choose the processor and the specific core on which a model is executed. This core-configuration can be applied to multiple Simulink models so that, for example, more than one model can run on the same core. By doing so, the user can specify an event for triggering one of the models: A time-based trigger to start after a specified time, or an update-trigger to begin when new data are available.

Furthermore, MATLAB's **external mode** can be configured, providing the ability to enable external mode simulations with FreeRTOS as an operating system on the Zynq hardware. The external mode simulation can also be used for RPU applications.



External mode data transfer

The **real-time communication** between models is realised with an Inter-Core Communication (ICC) manager and specified in a specification file. Once this file is loaded into Simulink, the SOK Zynq Target creates all necessary in- and outports in the Simulink model automatically. These in- and outports contain data which is combined in channels and transferred between different models. ICC can be used whether the models are running on the same core or on different cores.



Data transfer with two Simulink models and two Inter-Core Communication channels between them.

Moreover, the ICC manager enables a simple parameter management, since tuneable Simulink parameters are adjusted in a management model and then forwarded to user models.

A new and unique function of the SOK Zynq Target is to combine MATLAB with the Xilinx Vitis software: By specifying the path of a corresponding Xilinx Vitis project, the model is built externally by means of the **Xilinx Vitis build process**, without the need of exiting MATLAB. Subsequently, the code is deployed to the connected Zynq hardware and started automatically.

In addition to these new features, the SOK Zynq Target comes with different **Simulink library blocks** to support communication via various on-board or external protocols, e.g.

- **AXI** (bus protocol for communication with FPGAs)
- **Ethernet** (send/receive raw ethernet packages)
- **UDP**
- **CAN**.

Further protocols can be supported on request.

Links:

Produktseite
https://mathworks.com/products/simulink.html
https://www.xilinx.com/products/silicon-devices/soc/zynq-ultrascale-mpsoc.html